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Keryell, Ronan; Gozillon, Andrew; Harnisch, Gauthier; Kwon, Hyun; Chakaravarthy, Ravikumar; Wittig, Ralph

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SYCL for Xilinx Versal ACAP AIE CGRA

Andrew Gozillon1 Gauthier Harnisch1 Ronan Keryell1 Hyun Kwon1 Ravikumar Chakaravarthy1 Ralph Wittig2
1Xilinx 2University of the West of Scotland

Abstract

SYCL is a single-source C++ DSL targeting a large variety of accelerators in a unified way by using different backends. Xilinx Versal ACAP is a new system-on-chip (SoC) device integrating various computing resources like various CPUs, an FPGA, a coarse-grain reconfigurable array (CGRA), etc., interconnected by different network-on-chip (NoC).

The AIE CGRA is an array of 400 VLIW DSP operating on 512-bit vectors with their own neighborhood distributed memory (32 KiB data, 16 KiB instructions).

The SYCL implementation targeting the AIE CGRA by merging 2 different open-source implementations, geographical collective model.

The AIE CGRA is an array of 400 VLIW DSP operating on 512-bit vectors with their own neighborhood distributed memory (32 KiB data, 16 KiB instructions).

The SYCL device compiler generates LLVM IR for the Synopsys ASIP CHESS compiler generating the AIE instructions.

The host runtime runs on the ARM A72 CPU of the ACAP and controls the CGRA through the Xilinx libbsaiangine-v2 library.

CGRA architecture model and its SYCL model

First approach: expose geographical view of the chip

- Each tile is a sub-device with some neighborhood
- Can launch tasks on each tile
- Can use AIE-specific functions inside kernels
- Neighbor communications
- DMA
- Hardware locks
- Control of the AIE NoC done by host

SYCL with individual tile model: 1 tile = 1 sub-device

Second approach: entangled mode by weaving tiles and memories

- Plan SYCL can be commonplace with 400 tiles to program...
- Provide a cooperative mode allowing meta-programming tiles and memories
- Compile-time specialization of tiles (instructions) and memories (data)
- Allow each tile to access neighbor tile memories in a type-safe way

Weaving heterogeneous tiles and memories with meta-programming

Different multi-level implementation/emulation for hardware-software co-design

Implementation

Conclusion

Type-safe access to heterogeneous neighbor memories (PDE, stencil...)